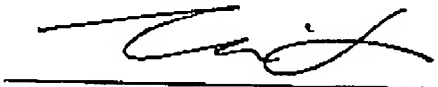
VERIFICATION OF TRANSLATION

I, Tetsu Yoshida, of Posz Law Group, PLC at 12040 South Lakes Drive, Suite 101, Reston, VA, 20191, do hereby state that I am competent in both Japanese and English, and that the attached document labeled Exhibit B is a true and accurate translation of the also attached document labeled Exhibit A to the best of my knowledge and belief.

Dated this 29th day of May, 2007

Signature: 

Tetsu Yoshida

Exhibit B

DENSO

To
TOYOTA MOTOR Co.
Second Electronic Technical Dept., 22nd e-room, Mr. Kondo. T
Second Electronic Technical Dept., 22nd e-room, Mr. Mori. T
Fourth Electronic Technical Dept., 41st e-room, Mr. Aoki T

AISHIN SEIKI Co.
Electronic Technical Dept., 1st e-group, Mr. Takeuchi
Element Tech-Development Dept., 2nd element development group, Mr. Goto
Braking System Development Dept., 2nd system group, Mr. Sakata T

IC of Unified Peripheral Devices for Standardized CPU Development Specification ABS-00-087 #4

DENSO Co. Safety Driving Technology, 4th Dept.		Approved		
		Reviewed		
		Drafted		
DATE of Issue JUN. 13. 2001	Safety & Chassis Syatems Eng. Dept. 4	No. ABS-00-087	1/	

Revisal Record

Marks	Date	Contents of Revisal
	2000/10/25	New Issue
#1	2000/11/21	Revisal of serial communication data bit table. Unite and disuse of flag portions in accordance with the revisal.
		(P.30, 35, 36, 36-2, 39, 40, 41, 42)
		Solenoid drive power monitoring logic (P.42)
		- disuse of leak monitor prohibit latch function during a ref. signal "fly-back"
#2	2000/12/13	P.7: Add note 1, add fVC5NG condition
		P.8: Add note 1, add fVC3NG condition
		P.9: Add fVSNNG condition
		P.13: Add details of input abnormal signal detection motions of a wheel rotation
		P.14-P.15: Add wheel rotation pulse check scheme plan
		P.16-P.20, P.22-P.24: Clarify I/F circuit inside IC for an application example
		P.18: Revise a typographical error in the title
		P.21: Add details of abnormal detection motion of oil

Exhibit B

		sensor with self-check function
		P.25-P.30, P.35: Revised table for true/false function value
		P.33: Add performance outline wave pattern, add Note1
		P.34: Revised performance outline wave pattern
		P.36: Revised performance outline wave pattern, add Note
		P.37: Add output frequency Q1 regulation P.39-P.42: Assign serial communication bits, change schedule
		(improve flexibility of software structure)
		P.43: Add communication scheme (plan)
		P.44-P.46: Monitor communication condition, add detailed explanation of communication condition monitoring
		P.51, Revise and add notes 1, 3
#3	2001/1/30	P.32: Add inside signal content explanation P.40: Revise data ID error, CPU -> IC , in communication schedule (two parts)
		P.41-P49: Divide a page of input/output data table
		P.42: Revise data ID errors (two portions)
		P.52: Note 3, add a bit replacement detail explanation
		Hereinafter, renumber page numerals
#4	2001/6/14	P17: 3 Threshold level VITHD1 of threshold input buffer, VITHD1 revised
		(correspondence with difficulty of changing chassis side FSW constant)
		P20: Revise open monitoring threshold level VIHANI of analog input buffer
		(correspondence to adjust a pressure sensor mode with a self-check function)
		P27, 41, 59: WTIR LED driver "active THILA" logic -> change to "passive THILA" logic
		However, possible to switch by a mask option (correspondence to a modification of system mode)
		P28, P29: Revise true/false function value table
		P40, 47, 48: Define serial communication data logic (the date being not in use), eliminate reference info. of active sensor
		P51, 52, 53: Revise typographical errors
		P60: Add a package outer shape
		P61: Change into a terminal arrangement final certified version

Exhibit B

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PAGE 3

3. Electronic Character / Thermal Character

[4] Wheel Velocity Input Circuit

(1) Wave Pattern Shaping Circuit

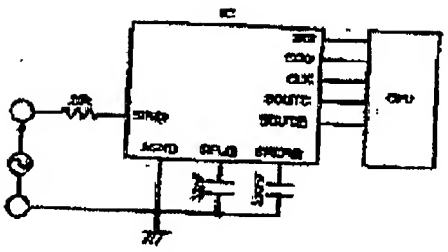
Voc=4V~VC5NGH, Tj=-40~150 °C unless particular instructions

Items	Marks	conditions	Min	Typ	Max	Unit
Input bias currency	ISIN@	VSIN=0.7 to 1.5V	-70	-50	-30	μA
Inside-resistance for a filter circuit	rSFL@		6	15	27	kΩ
	rSREF@		60	100	150	kΩ
Input clamp voltage	VCHSIN@	ISIN=5mA, SREF=1V	2.67	2.9	3.3	V
	VCLSIN@	ISIN=5mA, SREF=1V	-1.0	-0.7	-0.4	V
	VCHSFL1@	ISIN=5mA, SREF=1V	1.6	1.8	2.1	V
	VCHSFL2@	ISIN=5mA, SREF=2V	2.0	2.3	2.7	V
	VCLSFL@	ISIN=5mA, SREF=1V	0.2	0.4	0.6	V
Input sensitivity	VSEN1@	fIN=20Hz at test circuit	100	135	146	mVpp
	VSEN2@	fIN=60Hz at test circuit	106	143	156	mVpp
	VSEN3@	fIN=500Hz at test circuit	335	500	620	mVpp
	VSEN4@	fIN=1kHz at test circuit	645	980	1210	mVpp
	VSEN5@	fIN=2kHz at test circuit	1275	1945	2410	mVpp

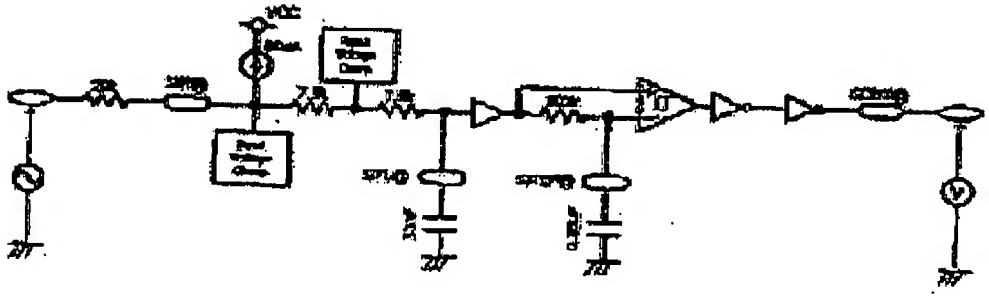
@=0,1,2,3

Exhibit B

Application circuit (example)



Test circuit



DATE of Issue OCT.25. 2000	Safety & Chassis Systems Eng. Dept. 4	No. ABS-00-087	11/

PAGE 4

3. Electronic Character / Thermal Character

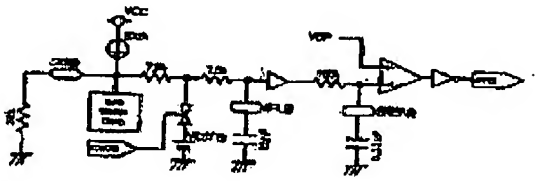
[4] Wheel Velocity Input Circuit

(2) Disconnection Monitoring Circuit, Capacitor Leak Check Circuit						
Voc=4V~VC5NGH, Tj=-40~150 °C unless particular instructions						
Items	Marks	conditions	Min	Typ	Max	Unit
Disconnection Monitoring Voltage	VOP@		1.6	1.8	2.1	V
Disconnection Monitoring Period	tSOF@		-	53	160	ms
Disconnection Monitoring Resistance	rSOP		1.3	16	52	kΩ
Clamp Voltage in a leak checking	VCSF@	ISIN=5mA to 5mA	2.3	2.55	2.7	V
Leak Monitoring Resistance	rLKCSFL		7	18	60	kΩ
	rLKCSREF		100	240	370	kΩ
Leak Monitoring	tCSF@	CSFL@=33nF CREF@0.33μF	-	40	160	ms

Exhibit B

Period						
@=0,1,2,3						

Logic



(3) Wave Pattern Shaping Output Circuit, Checking Output Circuit						
Vcc=4V~VCNGH, Tj=-40~150 °C unless particular instructions						
Items	Marks	conditions	Min	Typ	Max	Unit
H Level Output Voltage	VOHSOUT@ VOHSOUTC	IO=1mA	VCC -0.5	-	-	V
L Level Output Voltage	VOLSOUT@ VOLSOUTC	IO=1mA	-	-	0.3	V
@=0,1,2,3						

Check Output (SOUTC) Option Table

fSOCH	fSOCL	Output Channel
0	0	SOUT0
0	1	SOUT1
1	0	SOUT2
1	1	SOUT3

Output Status in a capacitor leak checking period

Output Channel	Output Status
SOUT0	H
SOUT1	L
SOUT2	H
SOUT3	L

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PAGE 5

【Wheel Velocity Input Malfunction Detection Process in details】

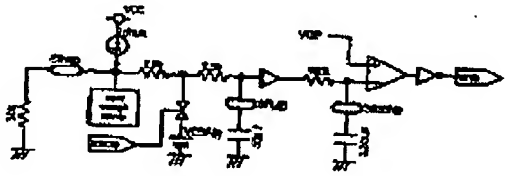
Detection of wheel velocity sensor disconnection

In case that a wheel velocity sensor is disconnected, a voltage raises by inside bias. In case that the wheel velocity sensor passes a threshold of a monitored disconnection, a flag (SF@)is set, then sent to CPU.

Capacitor Leakage Check

Exhibit B

In order to monitor a leakage of a capacitor used as a filter, a check requirement signal is received from CPU. Then, a certain voltage, which is more than disconnection monitored voltage, is applied in order to check whether there is a capacitor leakage or not.



Items		Min	Typ	Max
Disconnection Monitoring Resistance		1.3kΩ	16kΩ	52kΩ
Disconnection Monitoring Period			53ms	160ms
Disconnection Monitoring Period	SFL@side	7kΩ	18kΩ	60kΩ
	SREF@side	100kΩ	240kΩ	370kΩ
Leak Monitoring Period		-	40ms	160ms

*1 Disconnection and leak monitoring periods are greatly affected by internal resistance (100kΩ) and external capacitance (0.33μF). Therefore, it is possible to reduce a maximum monitoring period by using a high precision external capacitor.

*2 Disconnection Monitoring Period is defined as a period from a disconnection of input of SIN@ until a set of fSF@. Similarly, leak monitoring period is defined as a period from a set of fCKC@ until a set of fSF@. Accordingly, there is a certain delay for CPU, the delay which is derived from a communication schedule.

Check of interference of wave pattern shaping output

Detect interference between pins by stabilizing a status of each wave pattern shaping output while the above capacitance leakage check is activated.

Output Status during a capacitor leakage check

Output Channel	SOUT0 (fCKC0=1)	SOUT1 (fCKC1=1)	SOUT2 (fCKC2=1)	SOUT3 (fCKC3=1)
Output Status	H	L	H	L

Output for input capture check

Output a wheel rotation output from SOUTC which is selected by output channel selection signal that comes from CPU

Selection Signal	Output Channel

Exhibit B

fSOCH	fSOCL	
0	0	SOUT0
0	1	SOUT1
1	0	SOUT2
1	1	SOUT3

* IC also returns ISOCH and ISOCL. CPU receives that the output channel has been switched.

Wheel Velocity Pulse Check Scheme (plan)

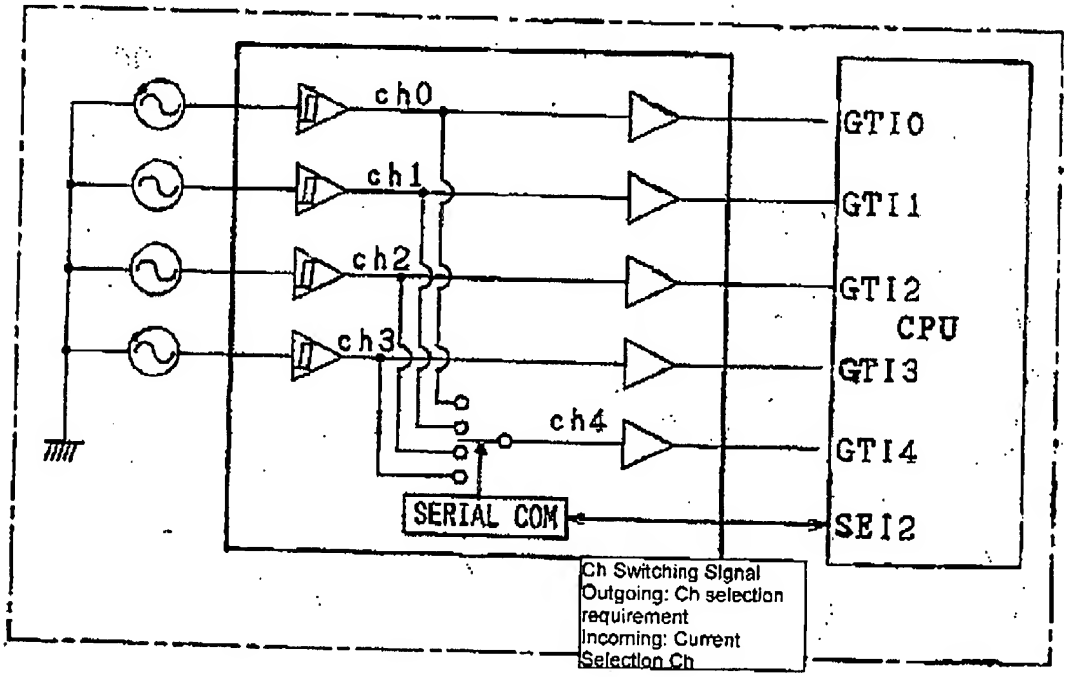


Exhibit B

(a flow chart on the left, top)
Software Process Images (plan)

PAGE 7

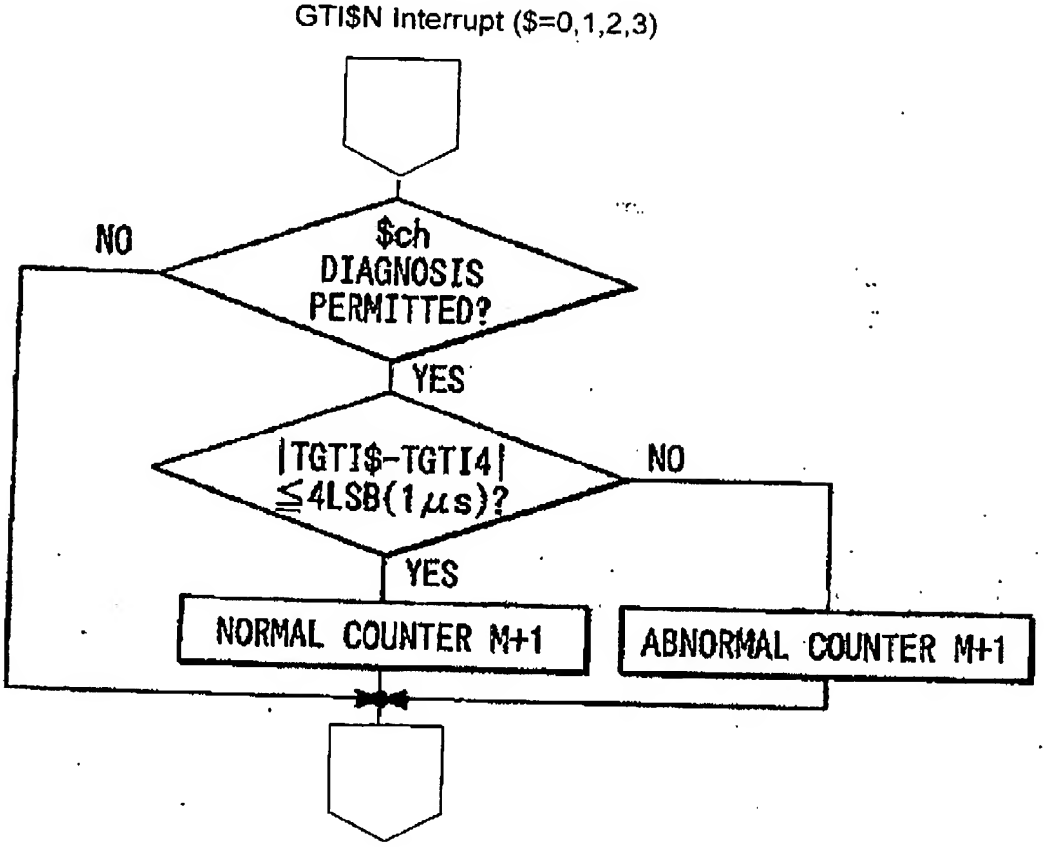


Exhibit B

(a flow chart on the right, top)

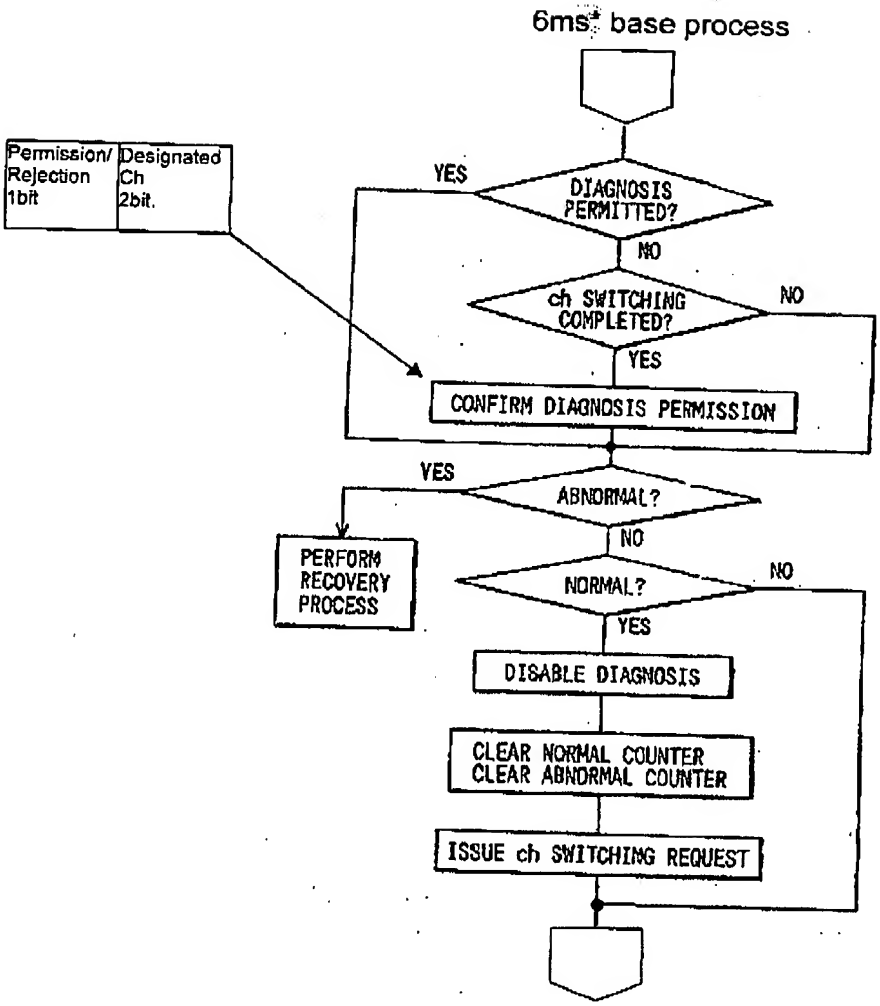
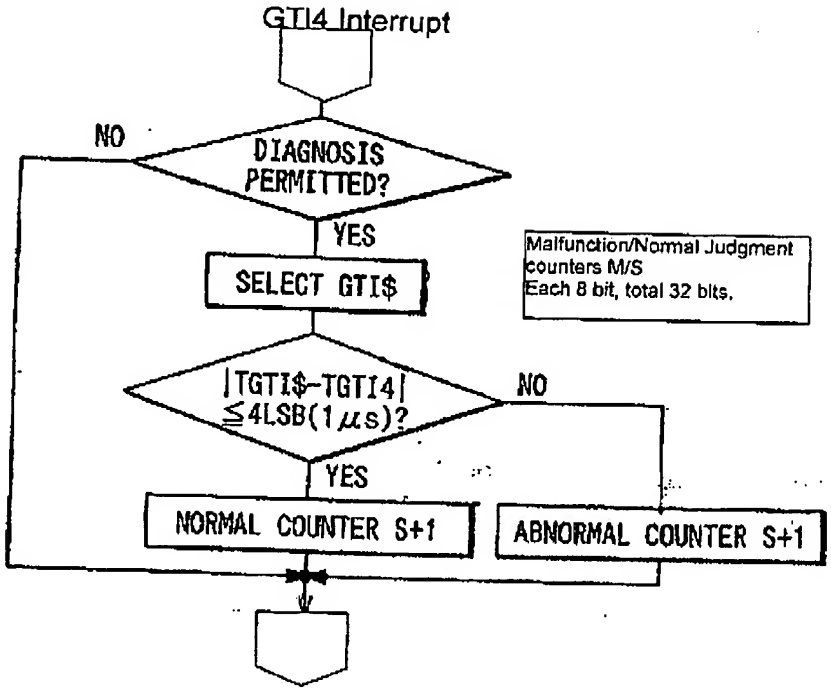


Exhibit B

(a second chart on the left)



Malfunction Judgment: A case is defined a malfunction where (1), (2), (3) all meet
(1) Malfunction Judgment Counter M > 1
(2) Malfunction Judgment Counter S > 3
(3) | Malfunction Judgment Counter M + Normal Judgment Counter M – Malfunction Judgment Counter S – Normal Judgment Counter S | > 3

Normal Judgment: A case is defined a normal where (1) and (2) both meet
(1) Normal Judgment Counter M>1
(2) Normal Judgment Counter S>1

DATE of Issue DEC. 13, 2000	Safety & Chassis Systems Eng. Dept. 4	No. ABS-00-087	15/

(1)

DENSO CORPORATION
1-1, Showa-cho, Kariya, Aichi 448-8661, Japan

ADDRESSEE

自動車㈱ TOYOTA MOTOR(CO.)
子技術部 ２２電子室 近藤T 殿
子技術部 ２２電子室 森T 殿
子技術部 ４１電子室 青木T 殿

ン精機㈱ AISHIN SEIKI (Co.)
系技術部 第一電子G 竹内 殿
技術開発部 第二要素開発G 技藤 殿
ーキシステム開発室システム第2G 坂田T 殿

資料

IC OF UNIFIED PERIPHERAL DEVICES FOR STANDARDIZED CPU

標準化ＥＣＵ用周辺機能統合ＩＣ

開発仕様書

ABS-00-087
#4

DEVELOPMENT SPECIFICATION

デンソー 技術4部	承認		
	検討		
	作成		

13,2001	Safety & Chassis Systems Eng. Dept.4	No. ABS-00-087	1/

DATE OF Issue

Exhibit A

(2) 1/1

DENSO CORPORATION
1-1, Showa-cho, Kariya, Aichi 448-8661, Japan

改訂履歴

記号	日付	改訂内容
	2000/10/25	新規発行
#1	2000/11/21	シリアル通信データビットテーブル見直し、それに伴いフラグ統廃合。 (P.30, 35, 38, 38-2, 39, 40, 41, 42)
		ソレノイド駆動出力モニタロジック (P.42)
		・非駆出力フライバック中のリークモニタ禁止ラッチ機能を廃止。
#2	2000/12/13	P.7: 注記1 追加、IVC5NG条件追加
		P.8: 注記1 追加、IVC3NG条件追加
		P.9: IVS1NG条件追加
		P.13: 車輪速入力異常検出動作詳細追加
		P.14~P.15: 車輪速パルスチェック方法変更追加
		P.16~P.20,P.22~P.24: アプリケーション例のIC内部VF回路明確化
		P.18: 表現固定訂正
		P.21: 自己診断機能付油圧センサ異常検出動作詳細追加
		P.25~P.30,P.35: 動作波形変更訂正
		P.33: 動作概略波形追加、注記1 追加
		P.34: 動作概略波形訂正
		P.36: 動作概略波形修正、注記追加
		P.37: 出力周波数01項目追加
		P.39~P.42: シリアル通信bitアサイン、スケジュール変更 (ソフトウエア構成のフレキシビリティ向上)
		P.43: 通信方法(案) 追加
		P.44~P.48: 通信状態監視、通信データ監視の詳細説明追加
		P.51: 注記3修正追記
#3	2001/1/30	P.32: 内部信号内容説明追加
		P.40: 通信スケジュール CPU→ICのデータID表記訂正(2ヶ所)
		P.41~P.49: 送受信データ定義表ページ分割
		P.42: データ内部表記訂正(2ヶ所)
		P.52: 注記3 加入停止詳細説明追加
		以降、ページ番号振り直し
#4	2001/6/14	P17: 3しきい値入力バッファのスレッショルドレベルVITHD1, VITLD41変更 (車両側FSW定数変更ができなかった為の対応)
		P20: アナログ入力バッファのオープン検出スレッショルドレベルVTHAN1変更 (自己診断機能付圧力センサ仕様変更への対応)
		P27,41,59: WIR LEDドライバー アクティブシラー論理→パッシブシラー論理に変更 但し、マスクオプションで切替可能 (システム仕様変更への対応)
		P28,P29: 動作波形波形訂正訂正
		P40,47,48: シリアル送信データ未使用論理の明確化、アクティブセンサ判定説明追加
		P51,52,53: 表記訂正
		P60: パッケージ外形形状追加
		P61: 端子部寸法許容差に変更

Date JUN.13,2001	Safety & Chassis Systems Eng. Dept.4	No. ABS-00-087	2/

DATE OF ISSUE

DENSO CORPORATION

3．電気的特性・熱的特性

1］車輪速入力回路

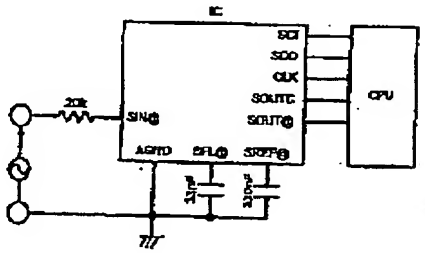
）波形整形回路

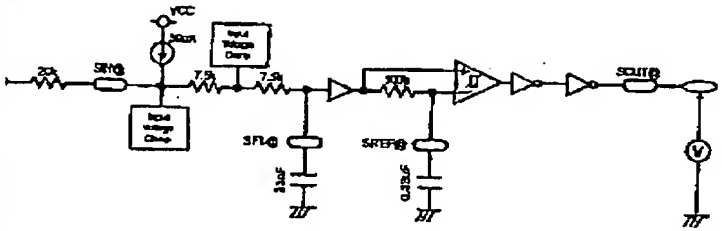
なき場合は Vcc=4V~VCSNGH, Tj=-40~150℃とする。

項目	記号	条件	Min	Typ	Max	単位
バイアス電流	ISIN@	VSIN=0.7 to 1.5V	-70	-50	-30	uA
ルタ抵抗用	rSFL@		6	15	27	kΩ
基板	rSREF@		60	100	150	kΩ
クランプ電圧	VCHSIN@	ISIN=5mA, SREF=1V	2.67	2.9	3.3	V
	VCLSIN@	ISIN=-5mA, SREF=1V	-1.0	-0.7	-0.4	V
	VCHSFL1@	ISIN=5mA, SREF=1V	1.6	1.8	2.1	V
	VCHSFL2@	ISIN=5mA, SREF=2V	2.0	2.3	2.7	V
	VCLSFL@	ISIN=-5mA, SREF=1V	0.2	0.4	0.6	V
感度	VSEN1@	fIN=20Hz at 試験回路	100	135	148	mVpp
	VSEN2@	fIN=80Hz at 試験回路	106	143	156	mVpp
	VSEN3@	fIN=500Hz at 試験回路	335	500	620	mVpp
	VSEN4@	fIN=1kHz at 試験回路	645	980	1210	mVpp
	VSEN5@	fIN=2kHz at 試験回路	1275	1945	2410	mVpp

@=0, 1, 2, 3

ケーション回路(例)





DATE OF ISSUE

DENSO CORPORATION

3．電気的特性・熱的特性

［4］車輪速入力回路

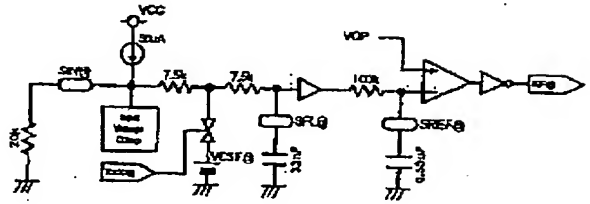
（2）断線検出回路、コンデンサリークチェック回路

指示なき場合は Vcc=4V~VCSNGH, Tj=-40~150℃とする。

項目	記号	条件	Min	Typ	Max	単位
断線検出電圧	VOP@		1.6	1.9	2.1	V
断線検出時間	tSOF@		-	53	160	ms
断線検出抵抗	rSOP		1.3	16	52	kΩ
リークチェック時クランプ電圧	VCSF@	ISIN=-5mA to 5mA	2.3	2.55	2.7	V
リーク検出抵抗	rLKCSFL		7	18	60	kΩ
	rLKCSREF		100	240	370	kΩ
リーク検出時間	tCSF@	CSFL@=33nF CREF@=0.33uF	-	40	160	ms

@=0, 1, 2, 3

Logic



（3）波形整形出力回路、チェック出力回路

指示なき場合は Vcc=4V~VCNGH, Tj=-40~150℃とする。

項目	記号	条件	Min	Typ	Max	単位
Hレベル出力電圧	VOHSOUT@ VOHSOUTC	IO=-1mA	VCC -0.5	-	-	V
Lレベル出力電圧	VOLSOUT@ VOLSOUTC	IO=1mA	-	-	0.3	V

@=0, 1, 2, 3

チェック出力(SOUTC)選択表

ISOCH	ISOCL	出力チャンネル
0	0	SOUT0
0	1	SOUT1
1	0	SOUT2
1	1	SOUT3

コンデンサリークチェック時出力状態

出力チャンネル	出力状態
SOUT0	H
SOUT1	L
SOUT2	H
SOUT3	L

DATE OF ISSUE

Exhibit A

Date of Issue

Exhibit A

= Fig. 1 of U.S. PATENT APPLICATION

DENSO CORPORATION

4/4

(17)

DENSO CORPORATION
1-1, Showa-cho, Kariya, Aichi 448-8661, Japan

ソフトウエア処理イメージ（案）

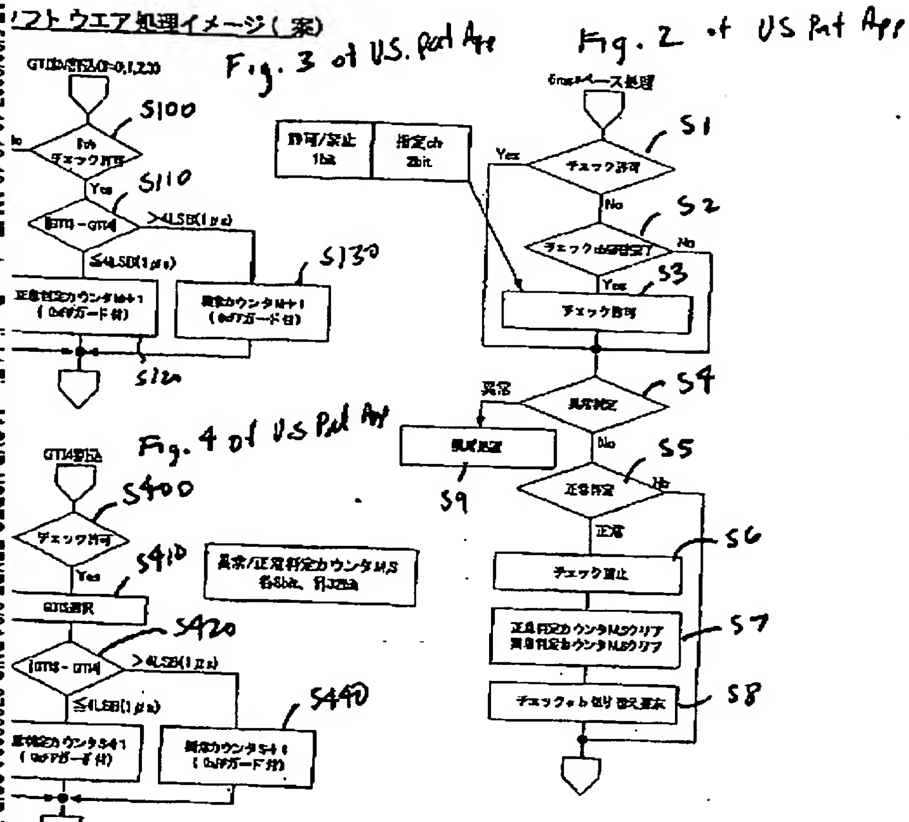


Exhibit A

判定 ： ①、②、③全て成立時異常と判定
①異常判定カウンタM>3
②異常判定カウンタS>3
③(異常判定カウンタM+正常判定カウンタM−異常判定カウンタS−正常判定カウンタS)>3

判定 ： ①、②全て成立時正常と判定
①正常判定カウンタM>1
②正常判定カウンタS>1

2000	Safety & Chassis Systems Eng. Dept.4	No. ABS-00-087	15/

↑ Date of Issue